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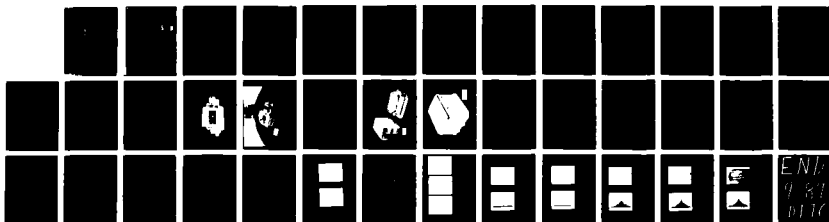
DUAL-GATE FET (FIELD EFFECT TRANSISTOR) AMPLIFIER
SWITCH TASK 1(U) DAVID SARNOFF RESEARCH CENTER
PRINCETON NJ D D HANSHINNEY 15 FEB 87 N00039-83-C-0131

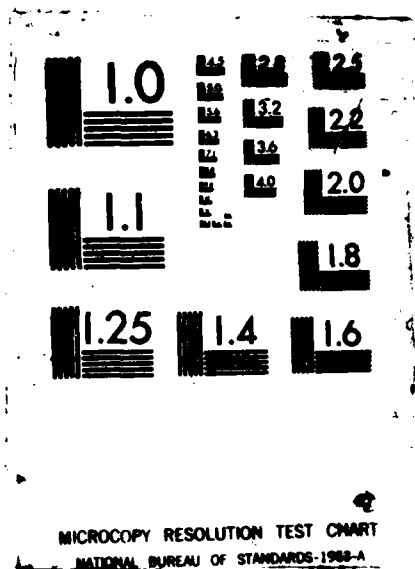
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**DUAL-GATE FET AMPLIFIER SWITCH
TASK I**

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15 February 1987

FINAL REPORT

for the period 1 January 1983 to December 1986

DISTRIBUTION STATEMENT A

Approved for public release
Distribution Unlimited

Prepared for
Naval Electronic Systems Command
Washington, DC 20363

Contract No. N00039-83-C-0131

87 4 28 132

REPORT 1

AD-A183 924^sForm Approved
OMB No. 0704-0188

1a. REPORT SECURITY CLASSIFICATION NONE			3. DISTRIBUTION/AVAILABILITY OF REPORT Commander Naval Electronic Systems Command (ELEX 00L) Washington, DC 20363-5100		
2a. SECURITY CLASSIFICATION AUTHORITY			5. MONITORING ORGANIZATION REPORT NUMBER(S)		
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE			7a. NAME OF MONITORING ORGANIZATION Naval Electronic Systems Command (ELEX 615)		
4. PERFORMING ORGANIZATION REPORT NUMBER(S)			7b. ADDRESS (City, State, and ZIP Code) Washington, DC 20363-5100		
6a. NAME OF PERFORMING ORGANIZATION RCA/David Sarnoff Research Ctr.		6b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER Contract N00039-83-C-0131		
6c. ADDRESS (City, State, and ZIP Code) P.O. Box 432 Princeton, NJ 08543-0432		8b. OFFICE SYMBOL (If applicable) N00039	10. SOURCE OF FUNDING NUMBERS		
8a. NAME OF FUNDING/SPONSORING ORGANIZATION Naval Electronic Systems Command		11. TITLE (Include Security Classification) Dual-Gate FET Amplifier Switch			
8c. ADDRESS (City, State, and ZIP Code) Washington, DC 20363-5100		PROGRAM ELEMENT NO.		PROJECT NO.	TASK NO. I
12. PERSONAL AUTHOR(S) Daniel D. Mawhinney		13b. TIME COVERED FROM Jan. 1983 TO Dec. 1986		14. DATE OF REPORT (Year, Month, Day) 1987/02/15	
13a. TYPE OF REPORT Final		15. PAGE COUNT		16. SUPPLEMENTARY NOTATION	
17. COSATI CODES		18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)			
FIELD	GROUP	SUB-GROUP			
19. ABSTRACT (Continue on reverse if necessary and identify by block number)					
<p>A gallium-arsenide dual-gate field effect transistor amplifier-switch was designed and fabricated to provide an improved means for generating a high-speed microwave pulse from a CW source to simulate an actual radar pulse. Fast rise and fall time capabilities was demonstrated by the FET amplifier-switches which provided an on-off ratio of more than 50-dB. Descriptions of the FET amplifier-switches are provided along with specific test results over the 7 to 11 GHz frequency range.</p>					
20. DISTRIBUTION/AVAILABILITY OF ABSTRACT <input type="checkbox"/> UNCLASSIFIED/UNLIMITED <input checked="" type="checkbox"/> SAME AS RPT <input type="checkbox"/> DTIC USERS			21. ABSTRACT SECURITY CLASSIFICATION NONE		
22a. NAME OF RESPONSIBLE INDIVIDUAL			22b. TELEPHONE (Include Area Code)		22c. OFFICE SYMBOL

PREFACE

This final report was prepared at the David Sarnoff Research Center, Princeton, New Jersey as a separate task under Contract N00039-83-C-0131. The report describes work performed on a developmental high-speed Dual-Gate FET Amplifier-Switch. The purpose of the switch is to generate a microwave pulse of controlled shape from a CW source to properly simulate a pulsed radar signal. The project engineer was D. Mawhinney, MTS, assisted by Senior Technical Associate, H. Milgazo, and was under the supervision of M. Nowogrodzki, Head of The Microwave Subsystems Group.

The problem of controlled simulation was brought to our attention by Mr. C.W. Wallace of the Naval Research Laboratory who provided assistance and direction in establishing the performance objectives. Mr. Temple Timberlake was the cognizant technical monitor and we appreciate the helpful guidance and counsel he provided.

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TASK I

DUAL-GATE FET AMPLIFIER-SWITCH

INTRODUCTION

The purpose of the gallium arsenide dual-gate field effect transistor (FET) amplifier-switch is to provide a means for high-speed switching of a microwave signal. One specific useage is the generation of simulated fast-rise-time-short microwave pulses, as might be produced by a high-resolution tracking or imaging radar transmitter, from a continuous-wave microwave source. This may be done with conventional high-speed PIN diodes but there are two potential limitations. First, the PIN-diode switch will have some attenuation that could be made up for by adding an amplifier stage. Second, as pointed out by Naval Research Laboratory personnel, the rise time of high-speed PIN-diode switches is defined as the time interval required for the switch output to change from 10% to 90% of full value. For most applications this may be adequate, but to simulate a sharp radar pulse the residual 10% represents a significant power level only 10 dB down from the maximum level. To adequately simulate a true full-off to full-on radar pulse, a 40-to 60-dB definition would be more appropriate.

The consequence of the less-than-adequate attenuation can best be demonstrated by considering the effect of the simulated pulse on a saturated receiver. This is shown, in somewhat exaggerated fashion, by Fig. 1. The simulated pulse is stretched by the saturated amplifier. In an extreme case, the cw nature of the source would be revealed and the pulse simulation would essentially fail.

The transmission characteristics of the dual-gate FET are controlled by the bias on the control gate which, unlike the PIN-diode, draws essentially no current and stores no charge. The control gate, if not capacitively bypassed,

can actually be used as a second microwave frequency (e.g., 10 GHz) input for mixing or modulation. As such, the bandwidth associated with rf pulses even as short as 10 ns (e.g., 100 MHz) can readily be accommodated. The control characteristics are such that the attenuation level will follow the input pulse, and equivalent rise times can be specified in terms of better than 1% to 99%. A much truer radar transmitter pulse simulation is expected to result. In addition, the dual-gate FET can provide some gain at the maximum control-gate voltage while the PIN-diode switch always has losses.

TECHNICAL RESULTS

During this program we developed a dual-gate FET amplifier-switch for evaluation and test. The program required delivery of one switch assembly, but to provide for a two-channel evaluation test system, two complete FET switch assemblies were fabricated, tested, and delivered for evaluation and use by Naval Research Laboratory personnel. The overall design, as shown in Fig. 2, consisted of two separately packaged dual-gate FET switch-amplifiers, each followed by a ferrite isolator, and an interlocked voltage regulator/pulse-driven printed circuit.

Each of the dual-gate FET amplifier stages used an NEC NE46,00 gallium arsenide FET in chip form with input and output microstrip matching sections fabricated on 0.025-inch-thick alumina substrates. The drain and signal-gate bias voltages were isolated via high-impedance choke lines and suitable rf bypass capacitors, and the control gate was bypassed with a 7-pF rutile capacitor to minimize pulse driver loading. The dual-gate FET is essentially a cascade arrangement of two single-gate FETs configured as shown in Fig. 3. All bias and pulse connections were made through low-capacitance hermetic feed-through pins soldered into the sides of the nickel-plated brass housing. A

photograph of the amplifier circuit before installation in a sealed housing is shown in Fig. 4.

The isolators were provided to minimize loading effects caused by the impedance mismatches at the FET input and output. These impedances vary as the control voltage is changed, and unpredictable oscillations and pulse distortions may occur unless adequate input and interstage isolation is provided. The isolators used in the FET amplifier-switch assembly were commercially available ferrite isolators, manufactured by UTE Microwave, that were rated to provide at least 18-dB isolation from 8-to 12-GHz. The physical layout of the two FET amplifiers and the two isolators is shown by the photograph of Fig. 5.

To simplify operation of the FET amplifier-switch, a printed circuit board with voltage regulators was also included. The NEC NE46300 FET devices required a drain voltage of +3 to +4 Vdc, a signal-gate bias of -1.0 Vdc, and a control-gate voltage from -4 to 0 Vdc for minimum to maximum output power. To protect the FET from a misapplication of voltages, the included regulator circuit (shown by the schematic of Fig. 6) includes overvoltage and reverse polarity protection diodes as well as an optically coupled interlock circuit that prevents application of the positive drain voltage unless the negative supply, needed for the signal-gate bias, is connected and turned on. The photograph of Fig. 7 shows the printed circuit board mounted in place over the microwave components. In the fully assembled form, the FET amplifier-switch is enclosed in the housing with access provided for mounting plate holes, as shown in Fig. 8.

Forward transmission gain measurements over the 7-to 11-GHz band were made by an automated network analyzer on both FET switch assemblies prior to delivery. Since the gain/loss characteristics vary with control-gate voltage, the measurements were made at several voltages, from zero to that required for maximum attenuation - nominally -3 to -4 V. These measurements are shown in

plotted format on Figs. 9 through 17 in accordance with the following tabulation:

FIG. NO.	FET SWITCH NO.	CONTROL-GATE BIAS (V)	NOMINAL GAIN/LOSS (dB)
9	1	0.0	+12
10	1	-1.7	- 2
11	1	-2.5	-22
12	1	-2.9	-44
13	2	0.0	+12
14	2	-1.7	+ 1
15	2	-2.5	-16
16	2	-3.0	-41
17	2	-4.0	-52

As may be observed from these data plots, a total power control range of more than 60 dB can be expected from each FET amplifier-switch with a control voltage swing from zero to -4 V. At zero bias, both assemblies have positive gain - a clear advantage over lossy PIN-diode switches. The effect of the input isolators can be observed from Figs. 18 and 19, which show the input VSWR of FET switches No. 1 and 2, respectively, at a control-gate bias of zero volt.

The basic capability of generating a microwave pulse from a cw source by the FET amplifier-switch is shown by the photographs of Fig. 20 for both a relatively long pulse (A) on the order of 5 μ s and a short pulse (B) of approximately 30 ns. These photographs were taken with various settings of the control voltage, demonstrating the potential power adjustment range of the FET amplifier-switch.

Switching speed measurements were somewhat restricted by available pulse

generators with limited rise times. In addition, it is difficult to measure a wide dynamic range response with a diode detector. To provide the capability of the FET amplifier-switch over a wide dynamic range, and comparing operation to PIN-diode switches, a microwave limiter amplifier was inserted ahead of a tunnel-diode detector to function as a saturated video detector. The test circuit, shown by Fig. 21, was used to evaluate the FET amplifier-switch and two commercial high-speed PIN-diode switches. The HP8734B PIN-diode switch driven by the HP8403A modulator has rise and fall times of approximately 25 ns and a full-off attenuation of more than 80 dB. Although the Alpha MT3086 PIN-diode switch, with a typical full-off loss of 75 dB, is rated for 10-ns rise and fall times, the pulse generator driver degrades both times to approximately 25 ns. The same pulse generator was used to drive the FET amplifier driver.

Comparative results are shown on Fig. 22 with the three switches driven by essentially the same pulse width. Both PIN-diode switches, the lower-isolation Alpha switch to a greater degree, show continuous output along the baseline (ripples) and a more distorted pulse than the FET amplifier-switch. The higher isolation (and more expensive) HP8734B PIN-diode switch shows less distortion than the Alpha but more than the FET amplifier-switch, which provides a good replica of a true on/off radar pulse as evidenced by the photographs of the spectra generated under various timing conditions shown in Figs. 23 through 27.

CONCLUSION

The use of dual-gate FET devices for on/off pulse simulation purposes will have advantages over PIN-diode switches because of the wide dynamic range and lack of charge storage. In addition, the FET switch can be designed to provide gain, whereas the PIN diode will have loss - possibly as much as 5 dB in the case of the HP8734B. Excellent control range characteristics are also available from the dual-gate FET amplifier-switch, which makes this switch suitable for

use as a high speed dynamic attenuator for pulse shaping or sensitivity time control applications.

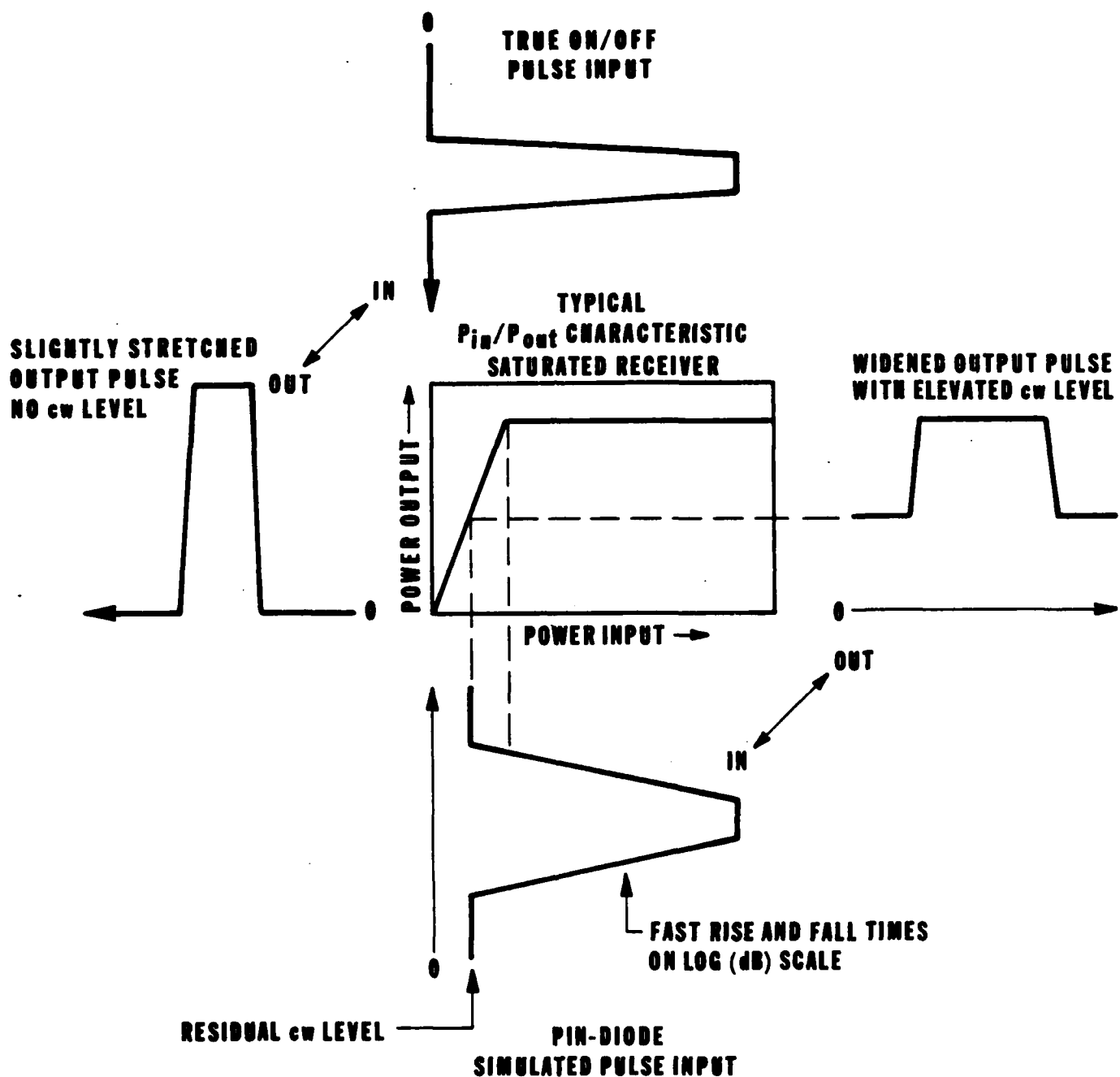


FIGURE 1. PULSE DISTORTION PRODUCED BY SATURATED RECEIVER ON PIN-DIODE SIMULATED RADAR TRANSMITTER PULSE.

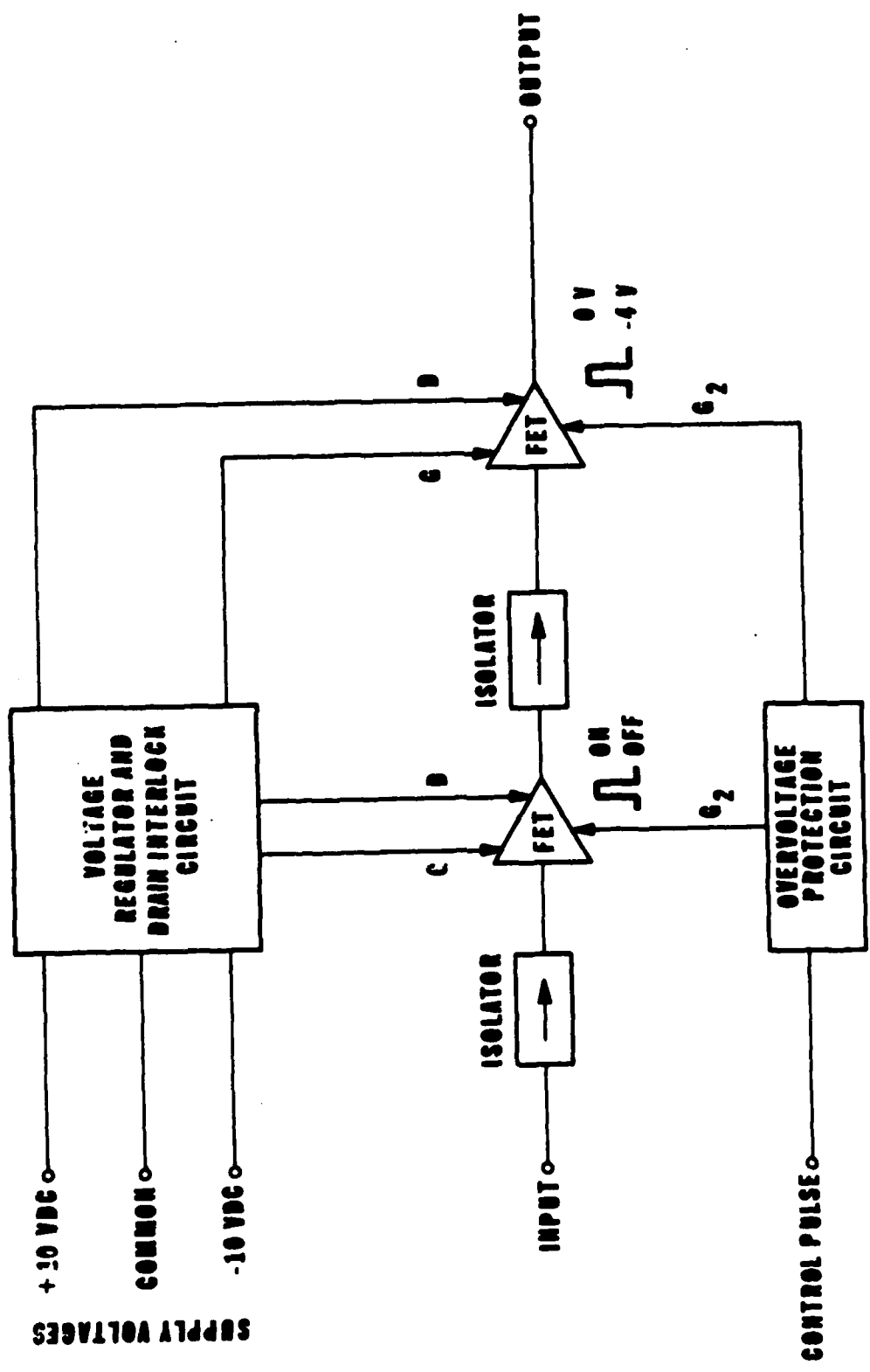
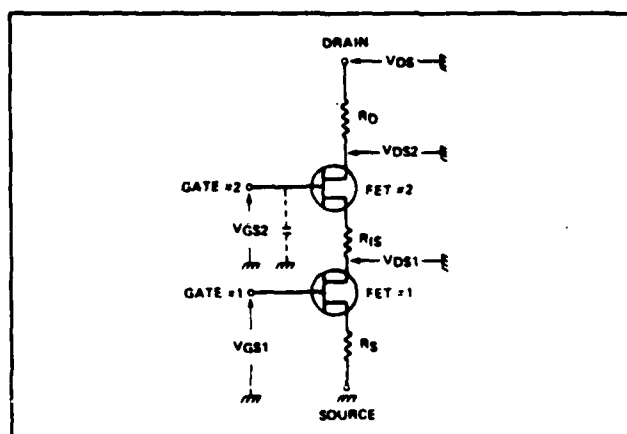


FIGURE 2. BLOCK DIAGRAM OF TWO-STAGE DUAL-GATE FET AMPLIFIER-SWITCH.

DEVICE CONFIGURATION



PHYSICAL DIMENSIONS (Units in mm)

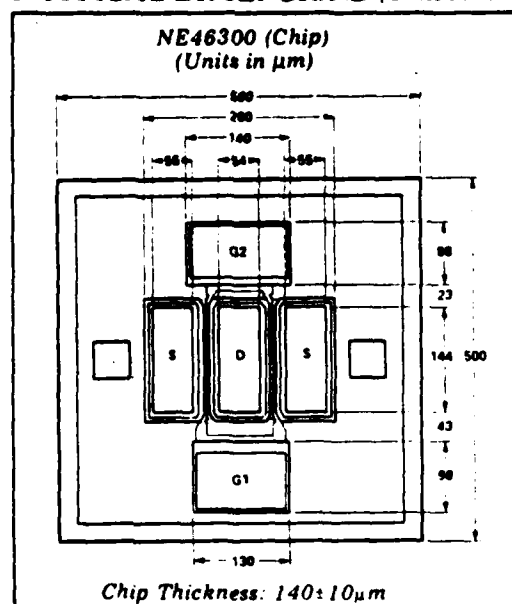


FIGURE 3. CONFIGURATION AND DIMENSIONS OF DUAL-GATE NE46300 FET CHIP.

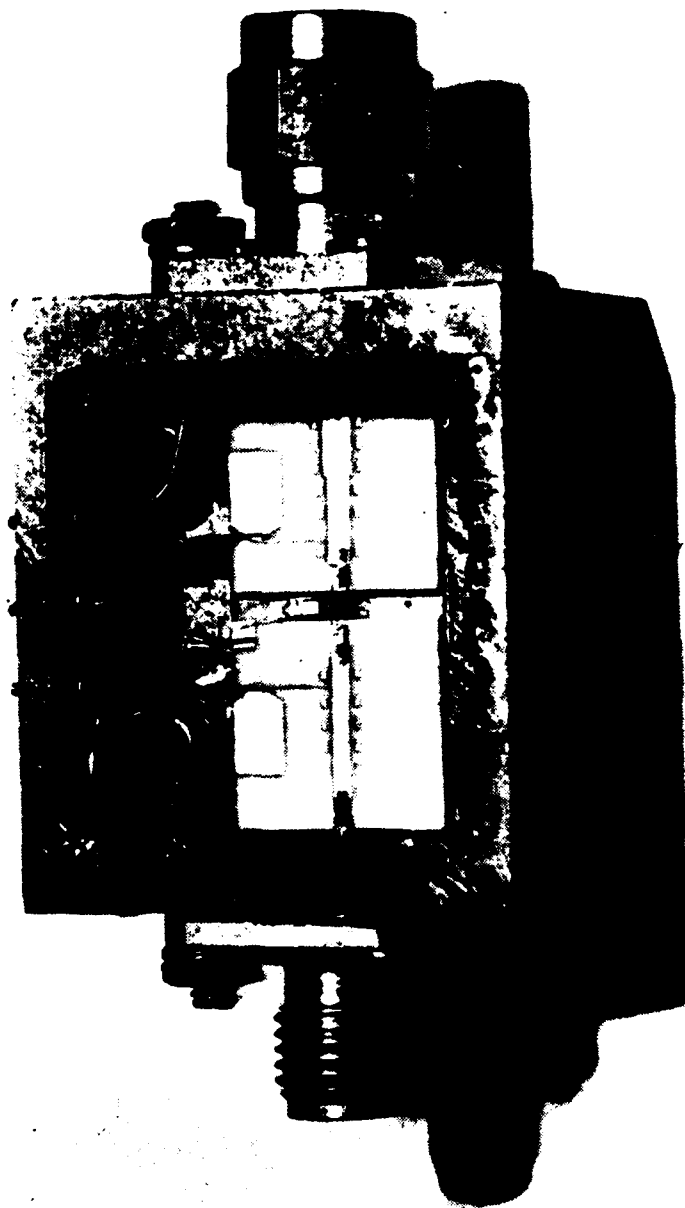


FIGURE 4. DUAL-GATE FET AMPLIFIER-SWITCH CIRCUIT.

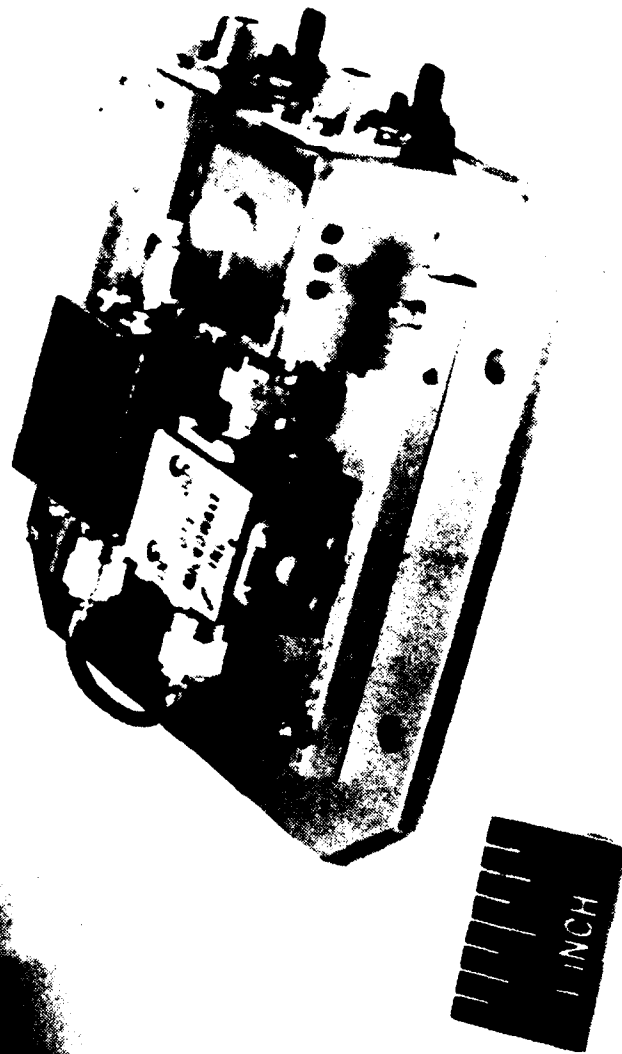


FIGURE 5. FET AMPLIFIER-SWITCH MOUNTED MICROWAVE COMPONENTS.

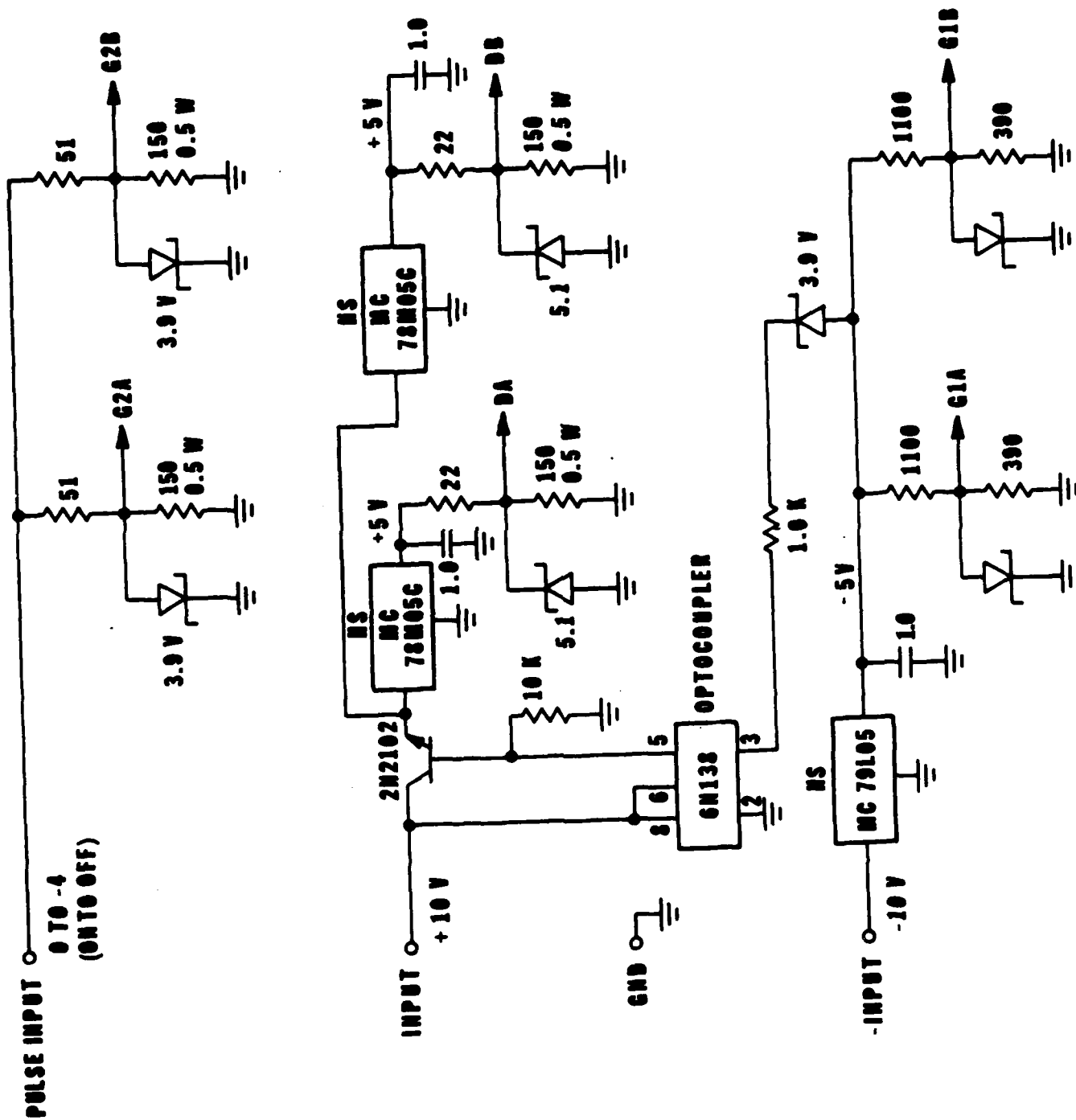


FIGURE 6. FET AMPLIFIER-SWITCH REGULATOR BOARD SCHEMATIC.

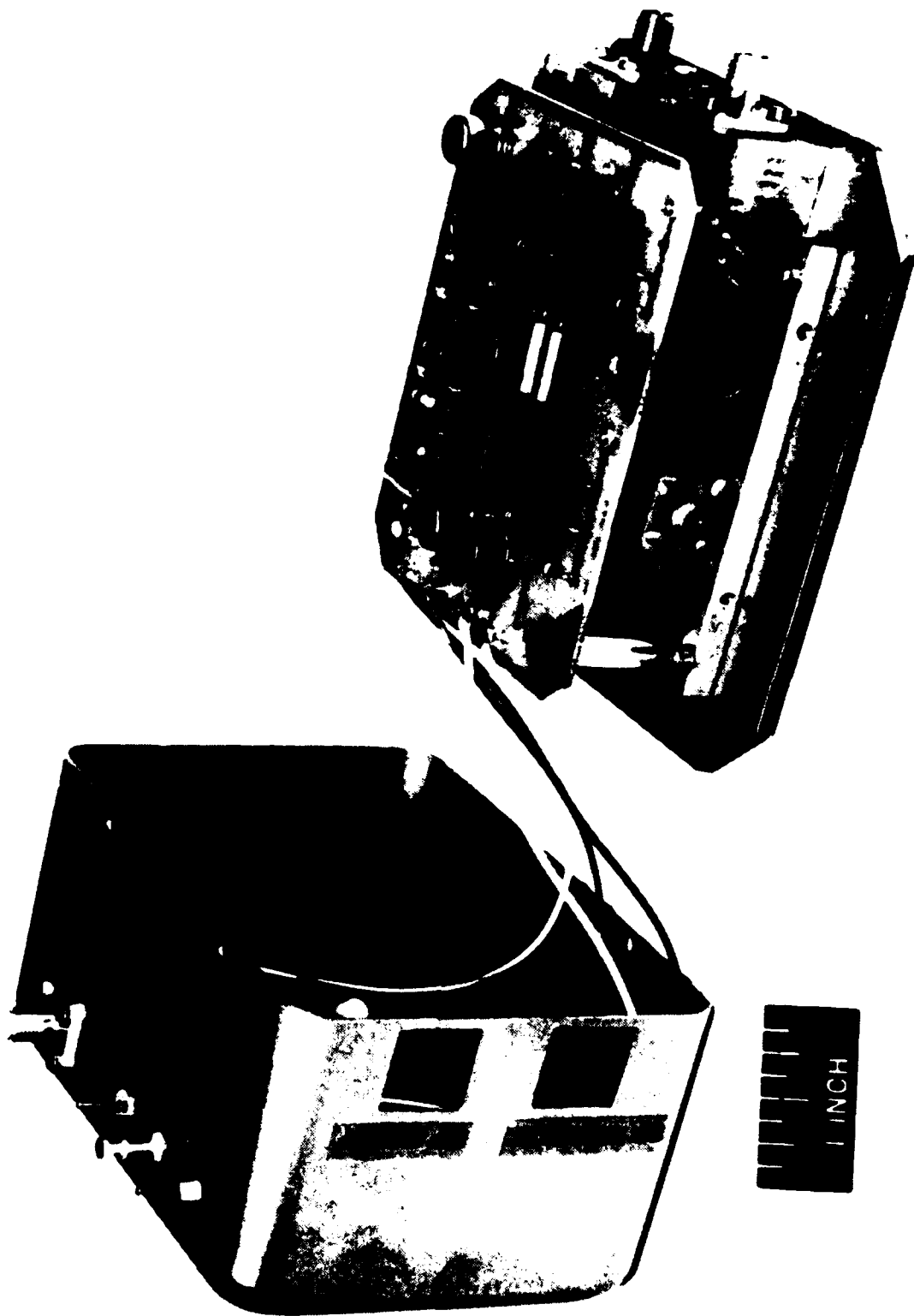


FIGURE 7. FET AMPLIFIER-SWITCH PARTIAL ASSEMBLY SHOWING VOLTAGE REGULATOR PC BOARD.

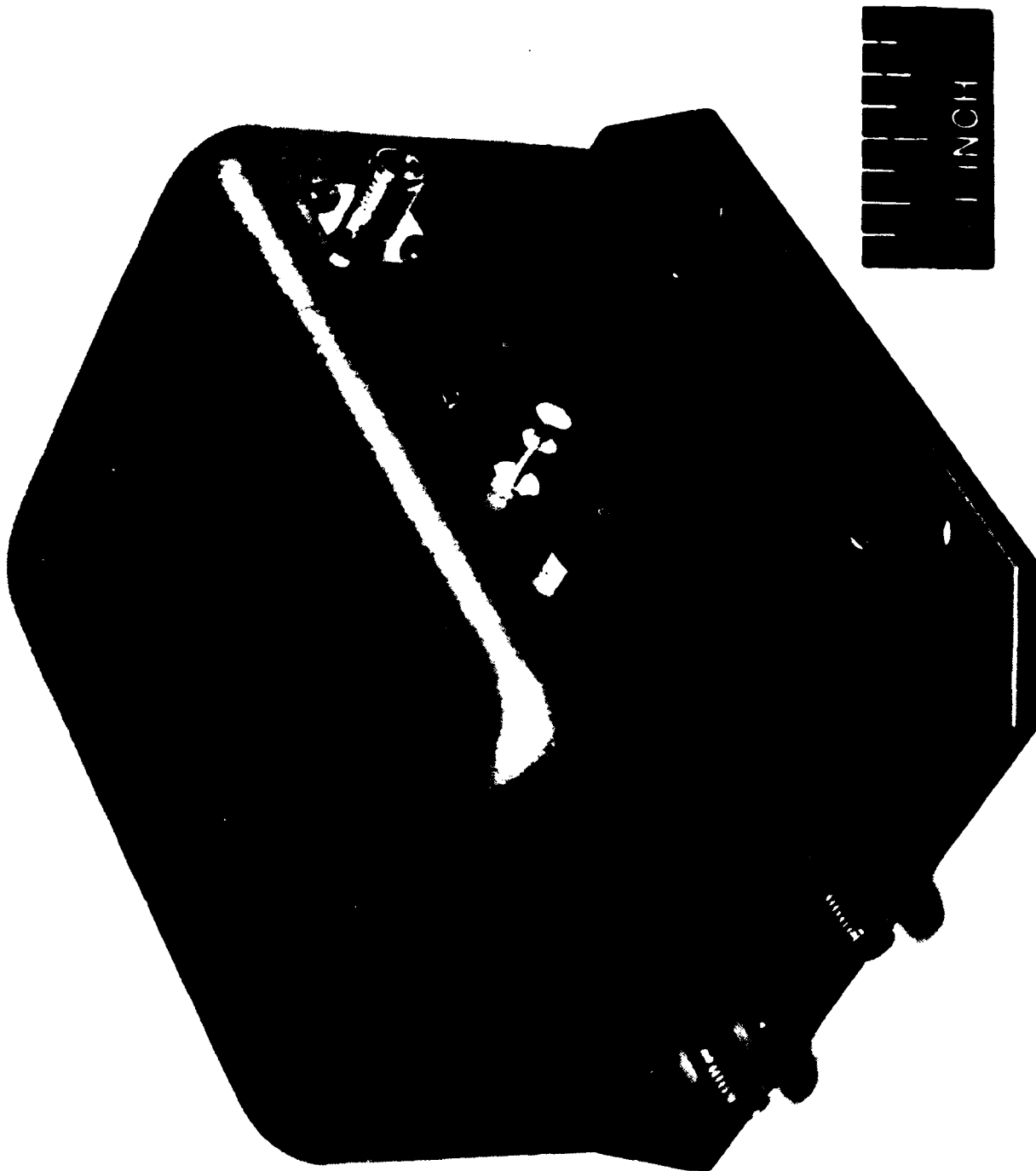


FIGURE 8. FET AMPLIFIER-SWITCH COMPLETE ASSEMBLY.

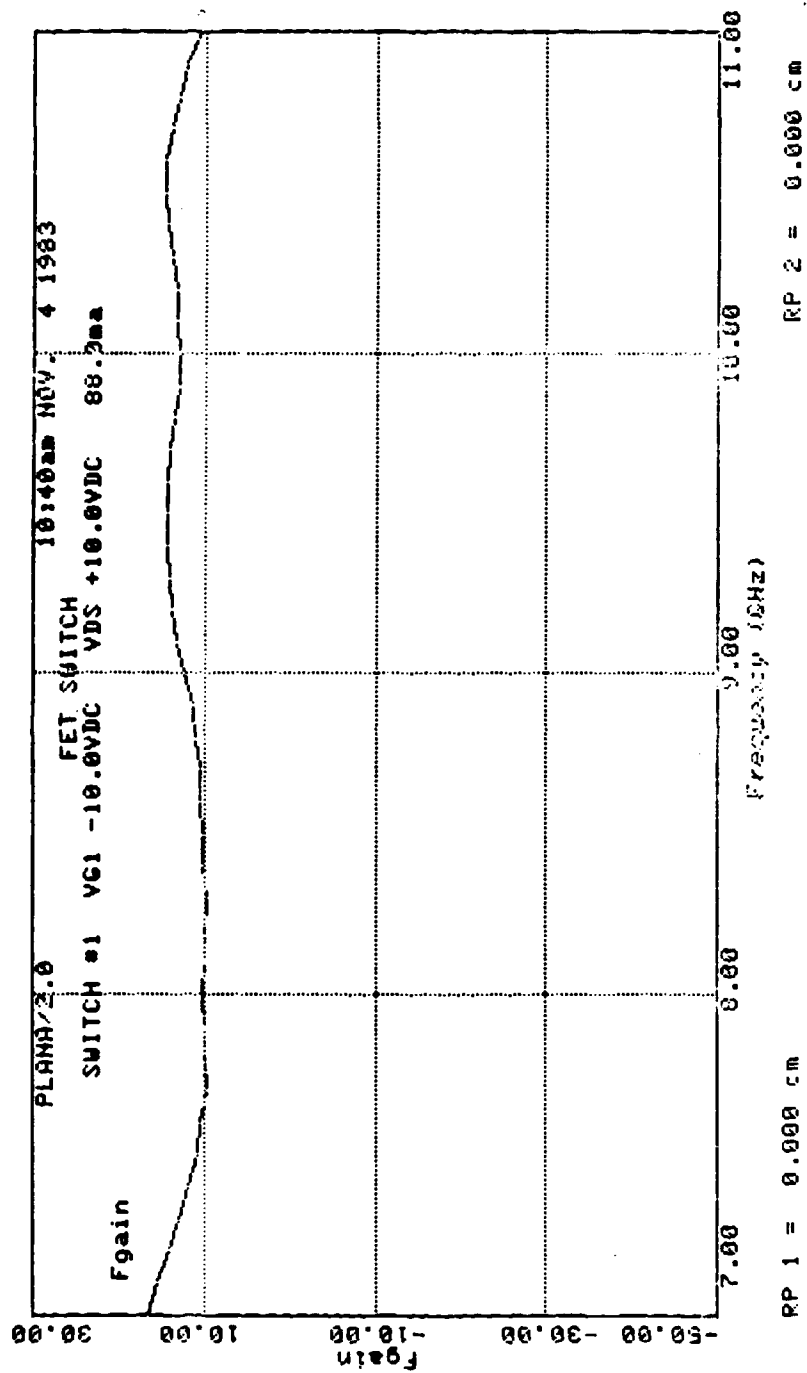


FIGURE 9. SWITCH NO. 1 WITH GATE AT 0.V

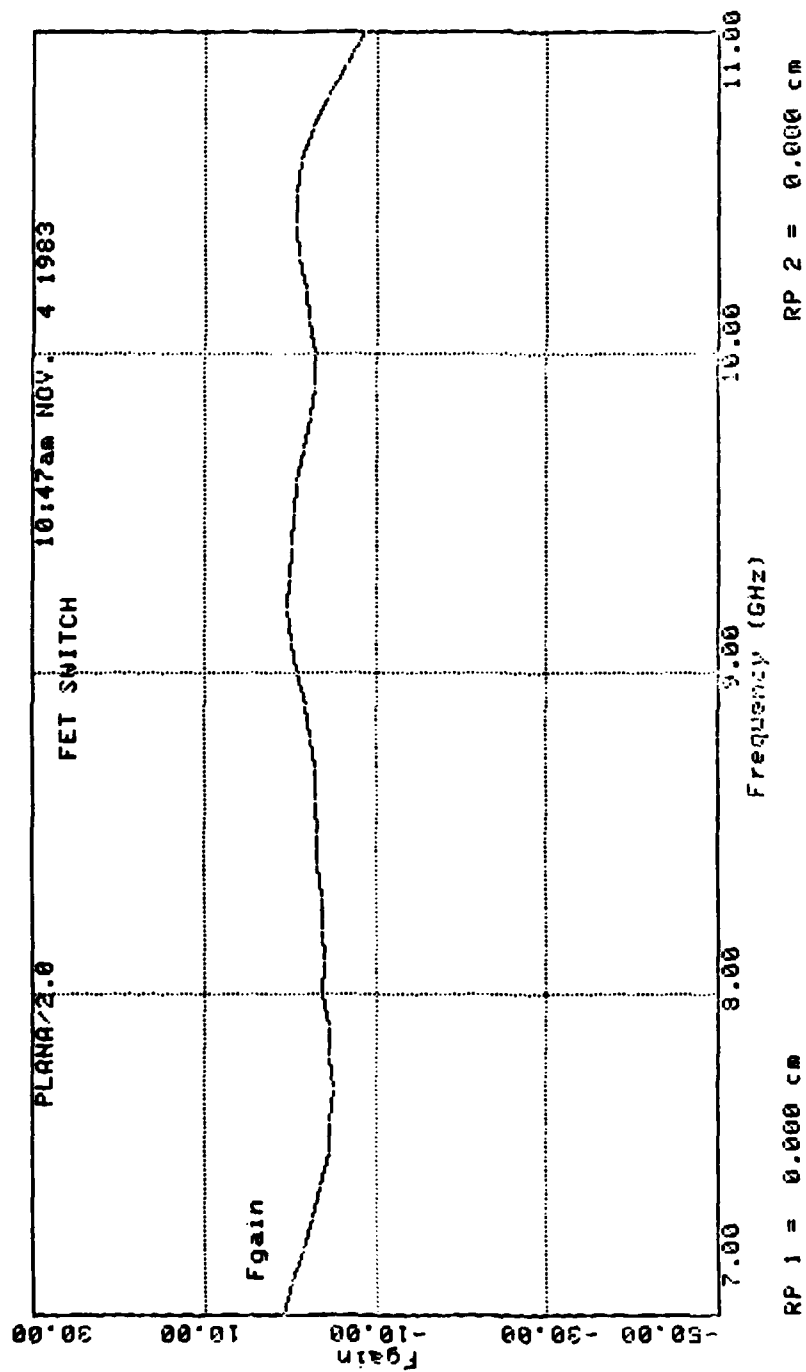


FIGURE 10. SWITCH NO. 1 WITH GATE AT 1.7 V

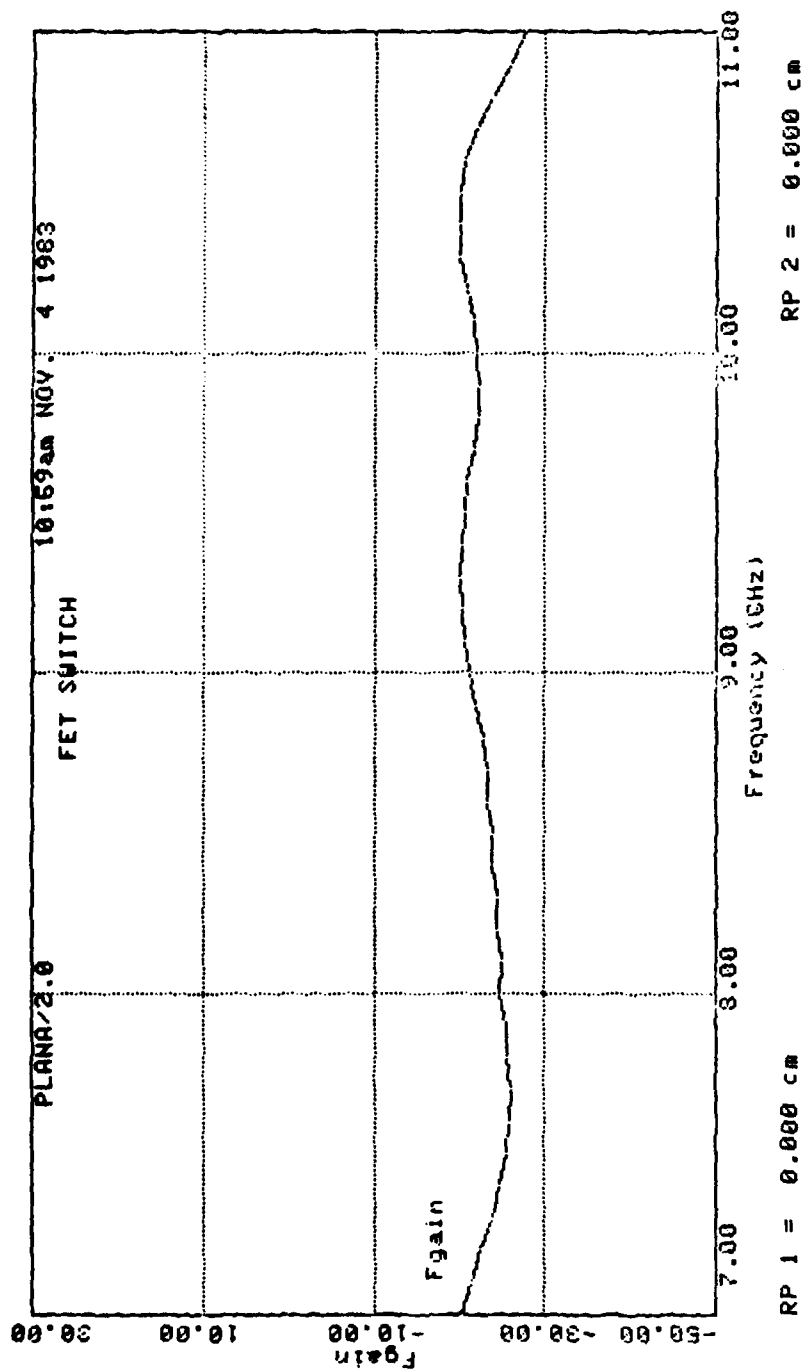


FIGURE 11. SWITCH NO. 1 WITH GATE AT 2.5 V

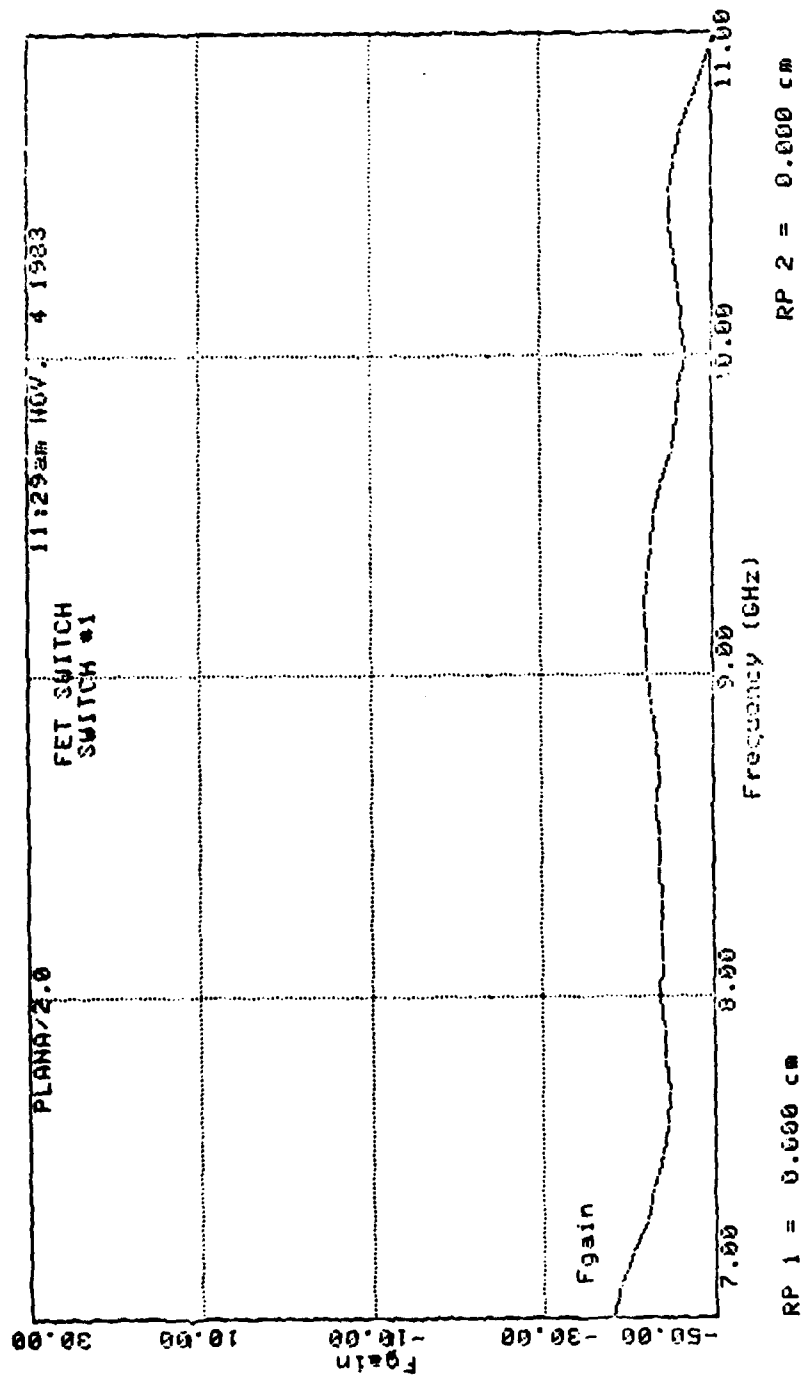


FIGURE NO. 12. SWITCH NO. 1 WITH GATE AT 2.9 V

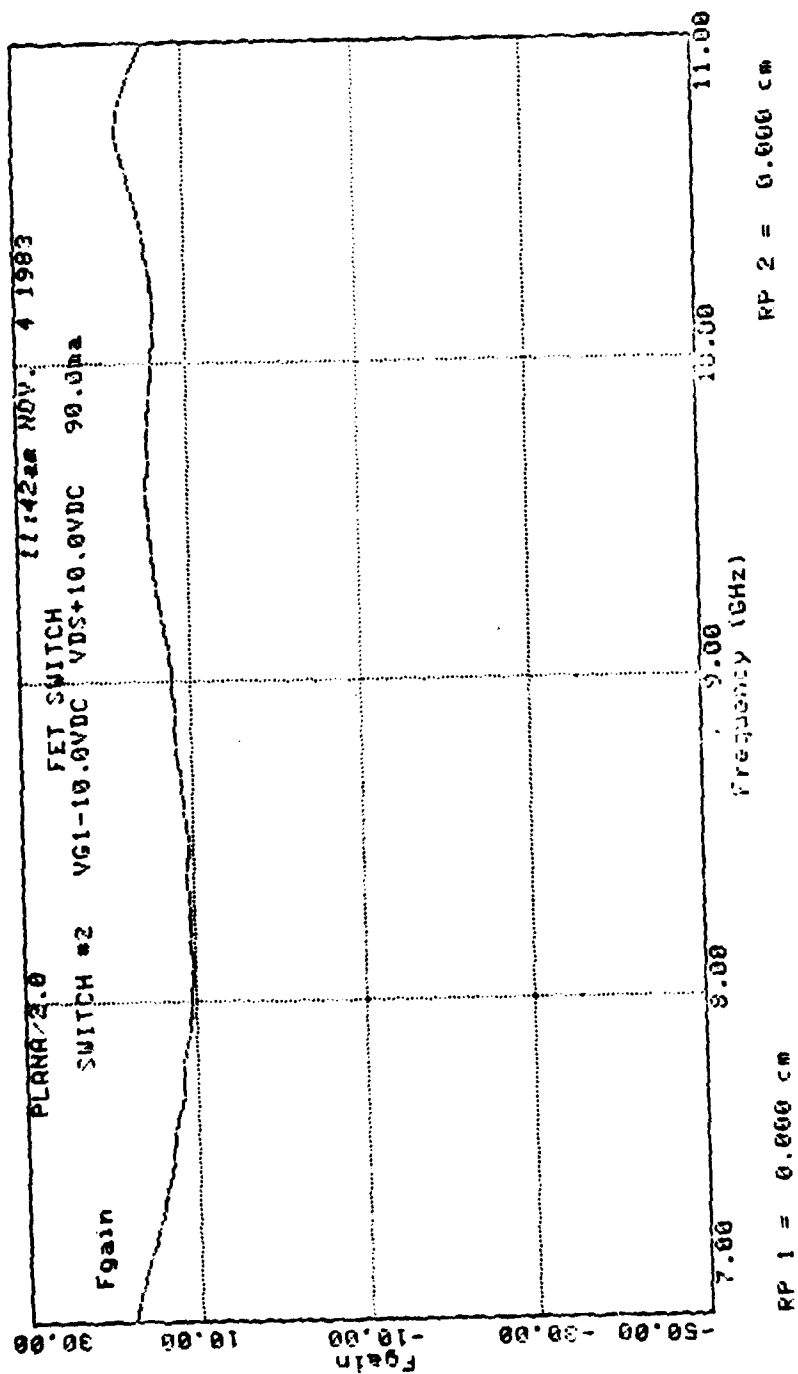


FIGURE 13. SWITCH NO. 2 WITH GATE AT 0 V

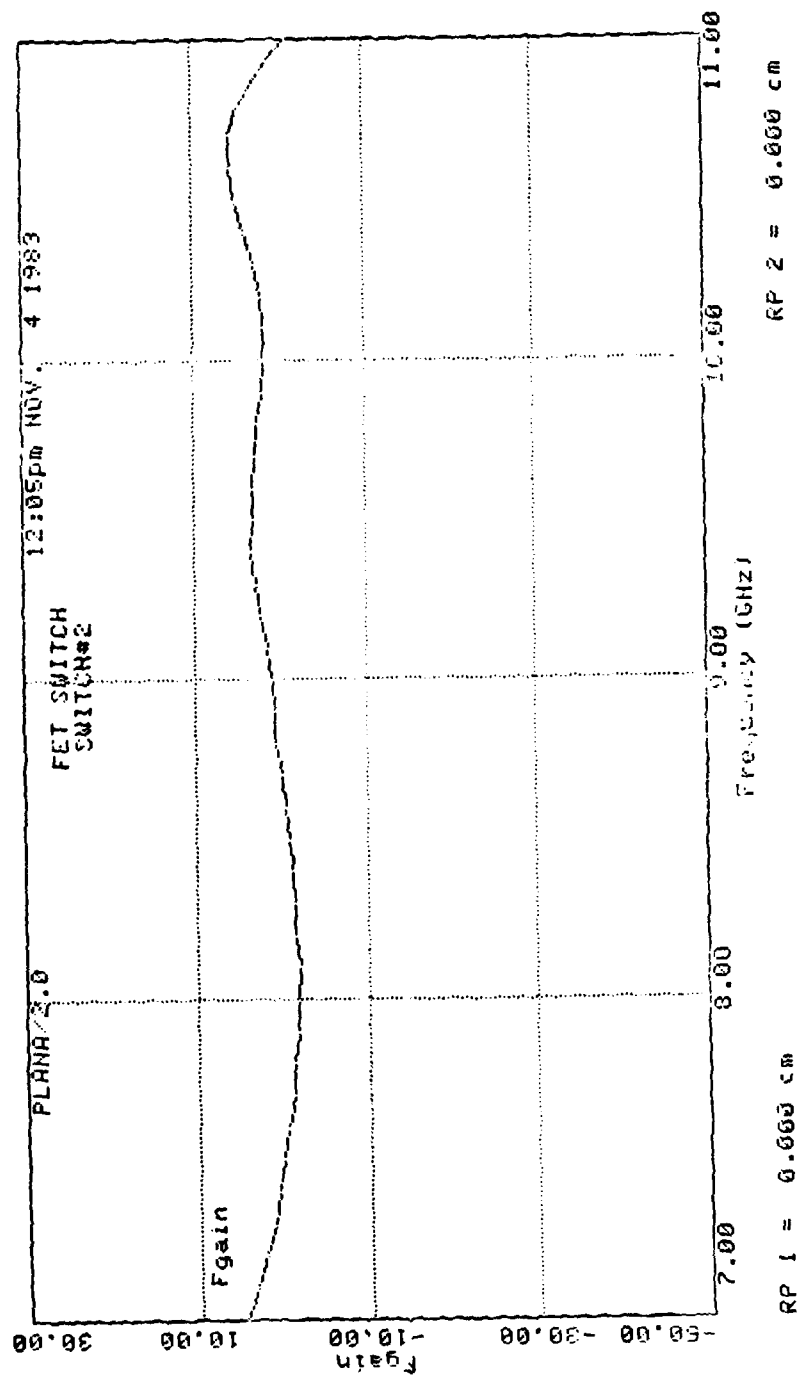


FIGURE 14. SWITCH NO. 2 WITH GATE AT 1.7 V

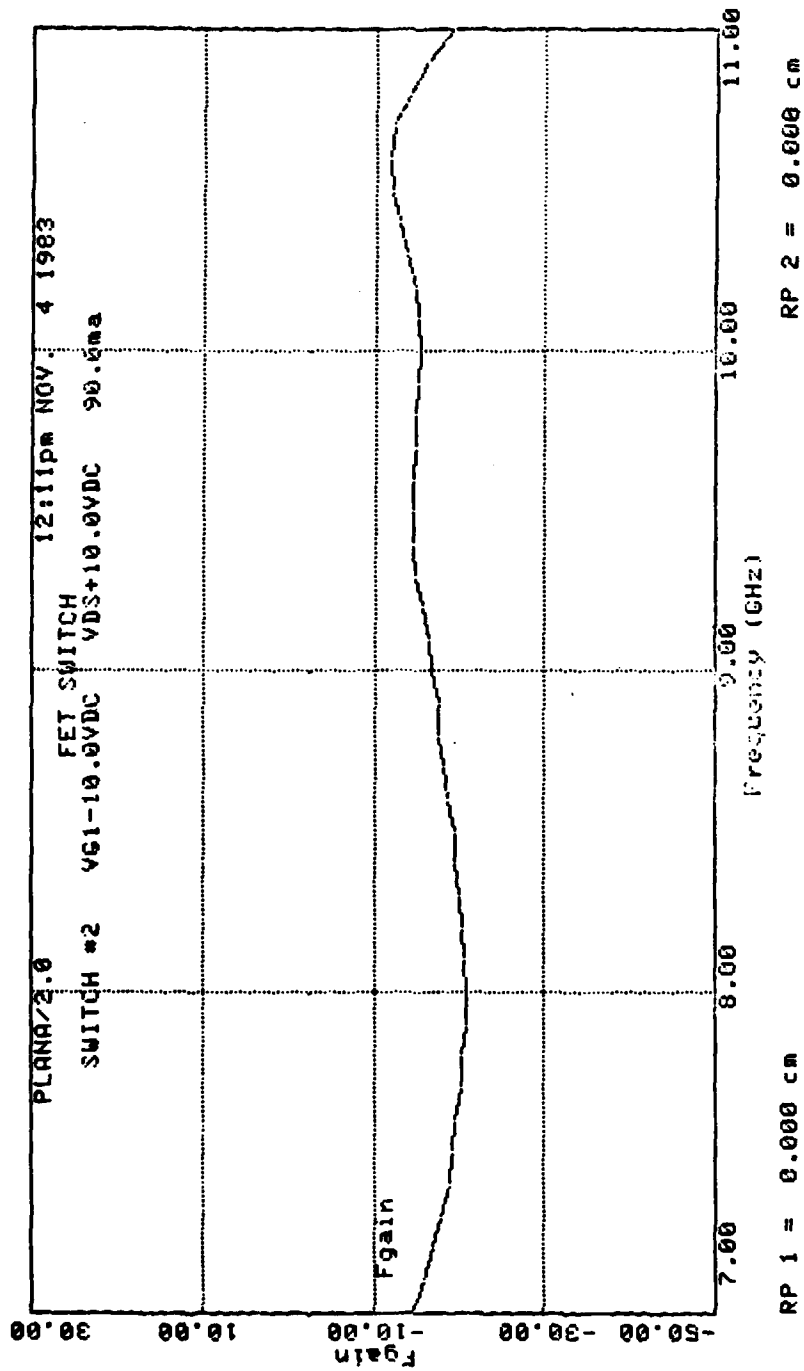


FIGURE 15. SWITCH NO. 2 WITH GATE AT 2.5 V

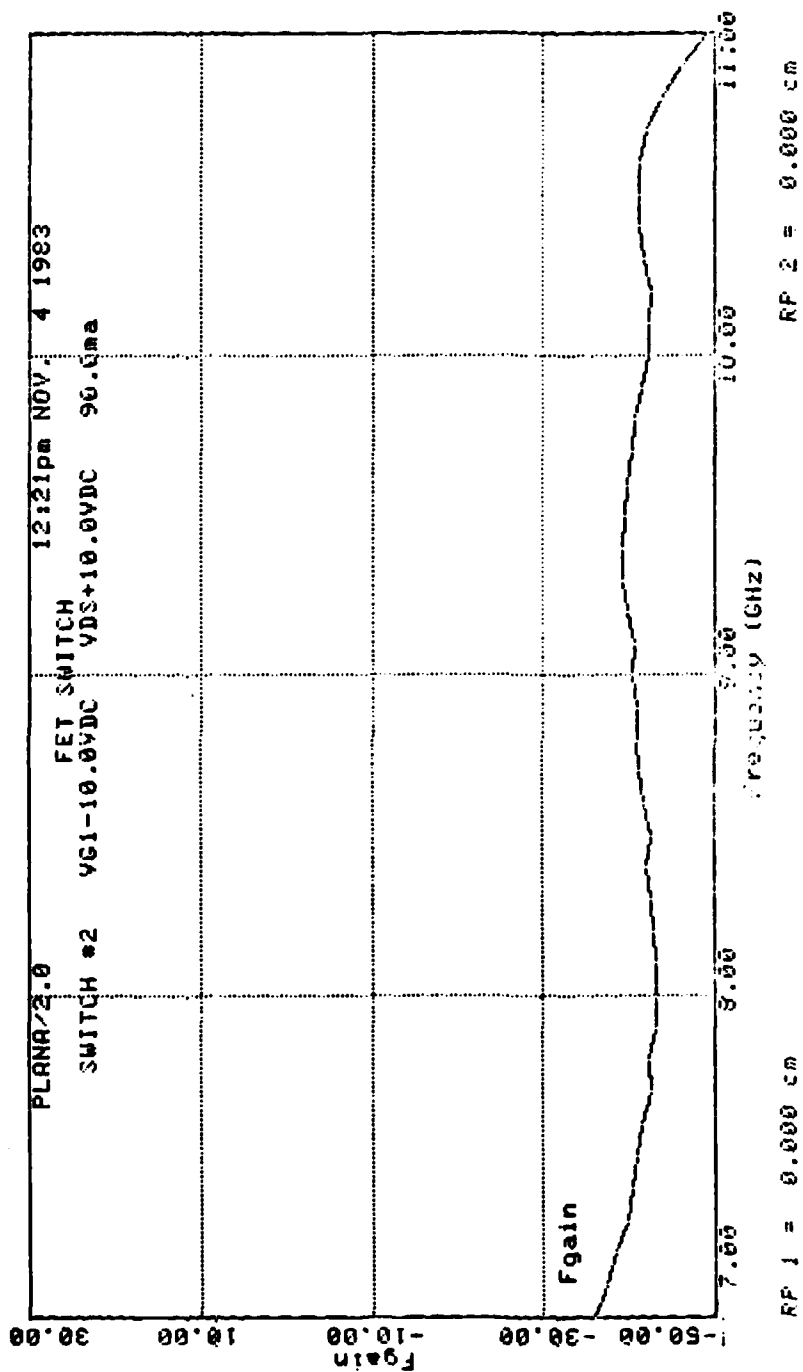


FIGURE 16. SWITCH NO. 2 WITH GATE AT 3.0 V

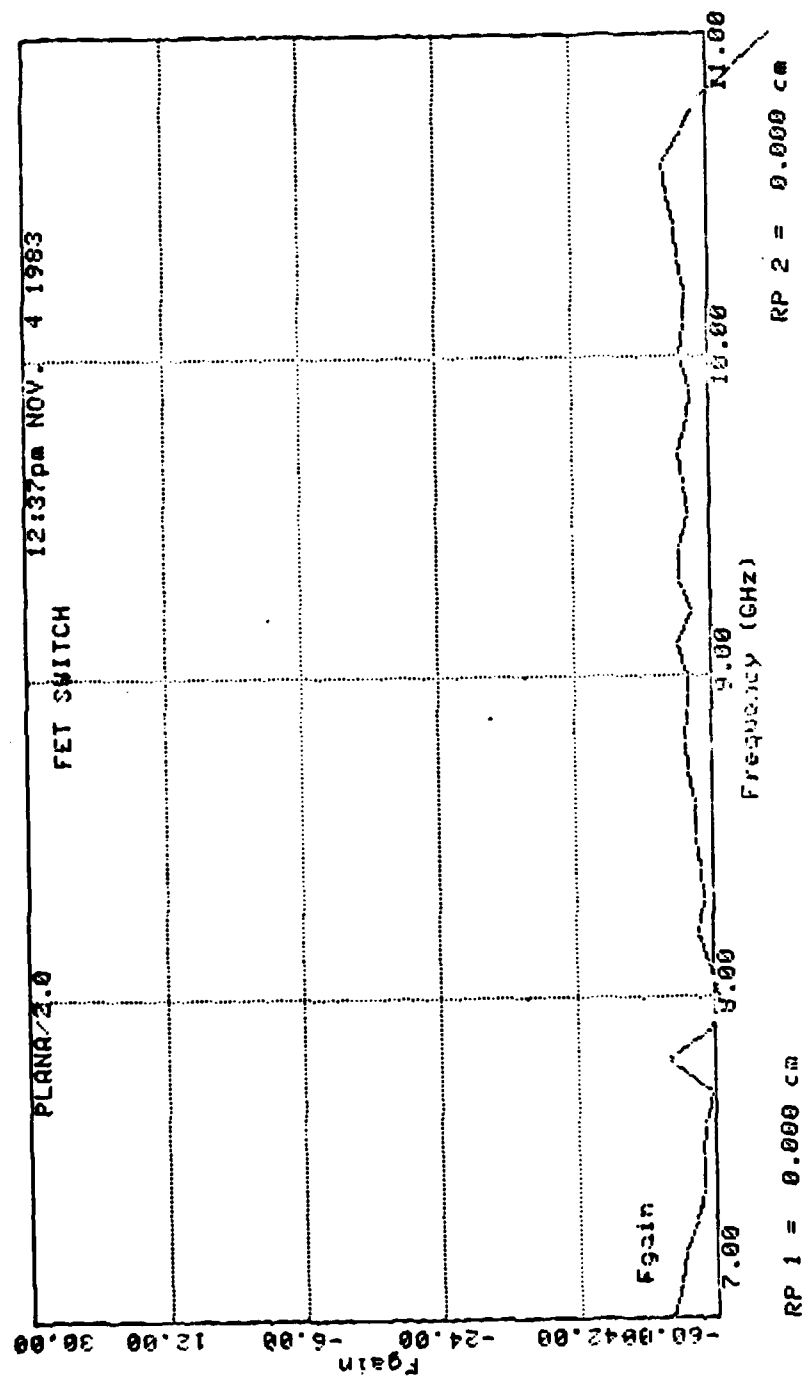


FIGURE 17. SWITCH NO. 2 WITH GATE AT 4.0 V

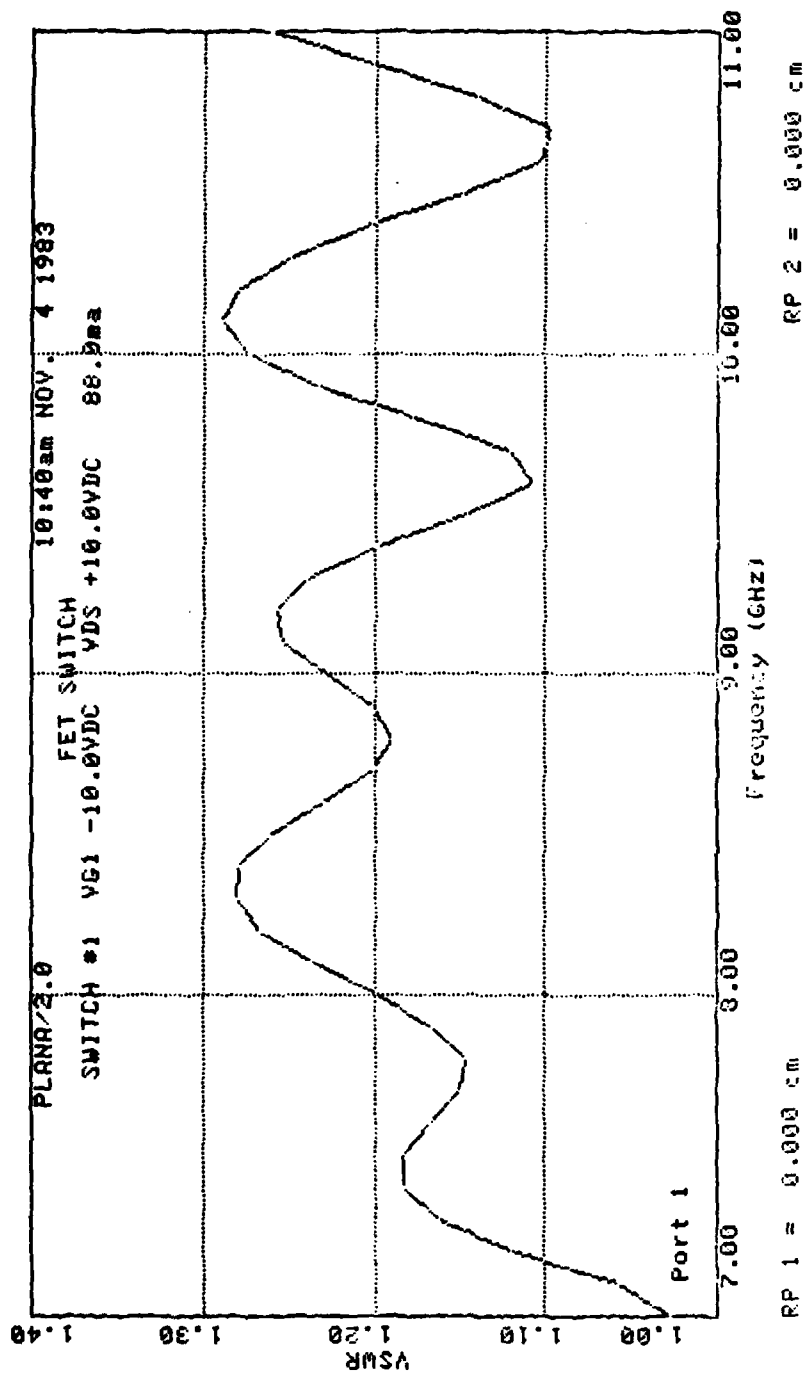


FIGURE 18. SWITCH NO. 1 - INPUT MATCH

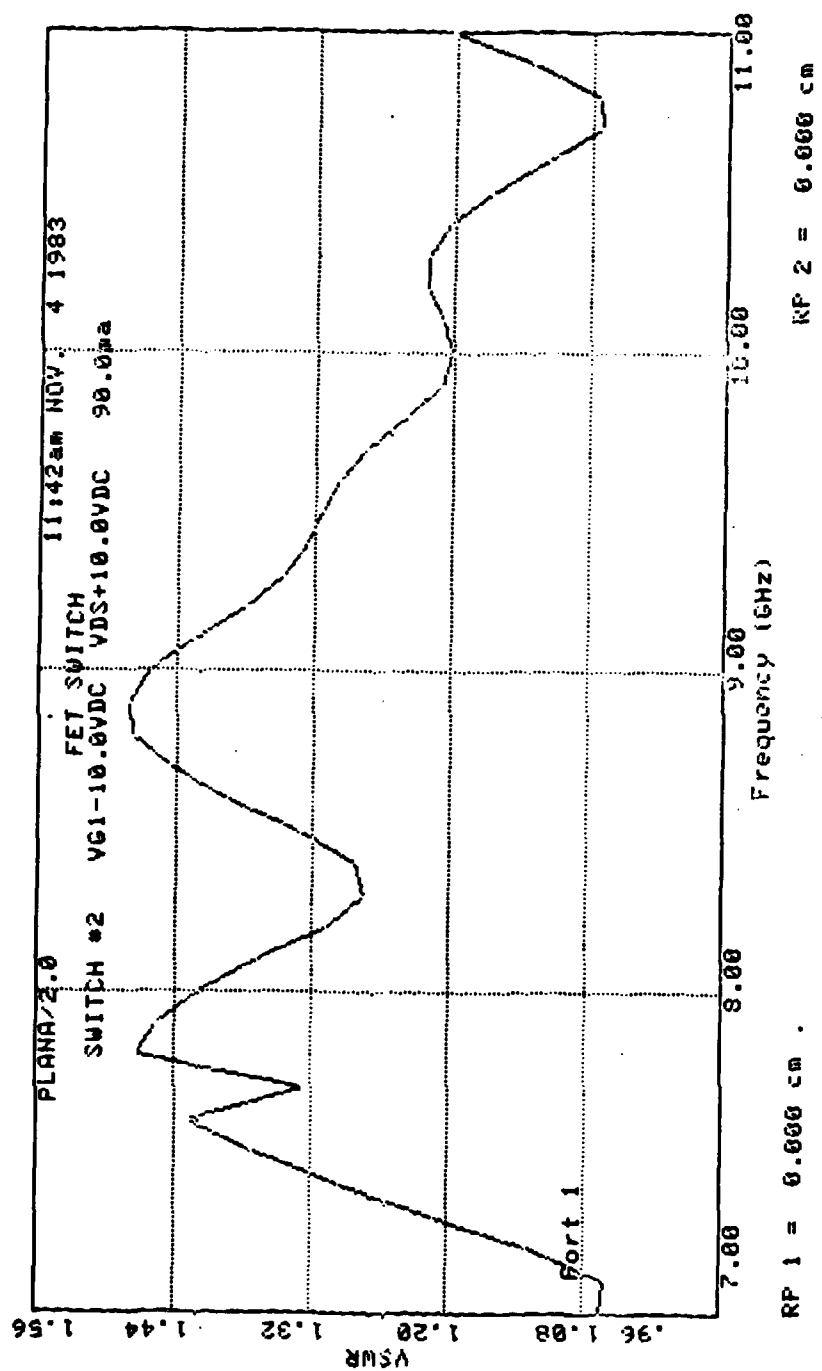
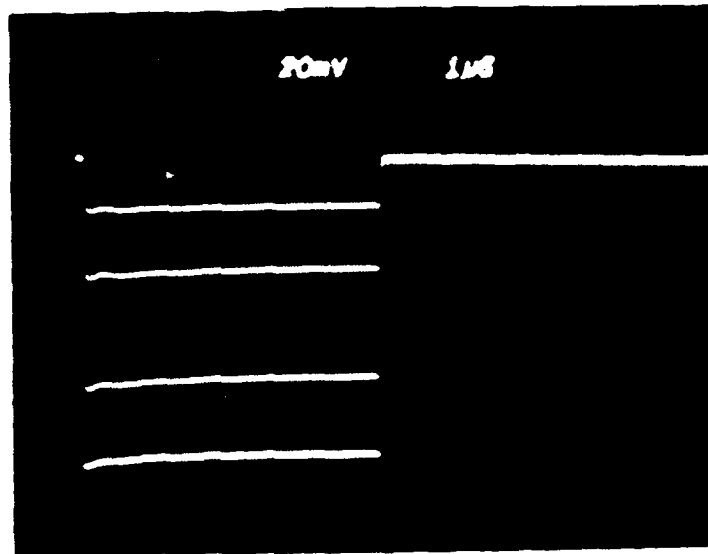
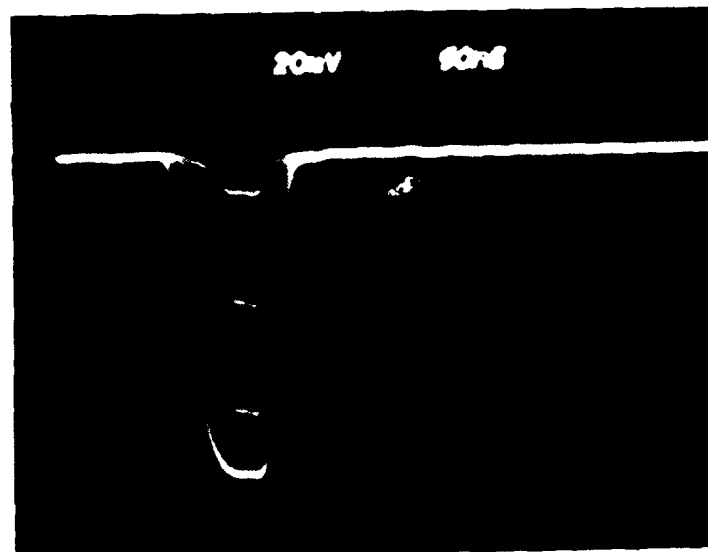


FIGURE 19. SWITCH NO. 2 - INPUT MATCH



A



B

FIGURE 20. LONG- AND SHORT-PULSE GENERATION OBTAINED WITH THE FET AMPLIFIER-SWITCH.

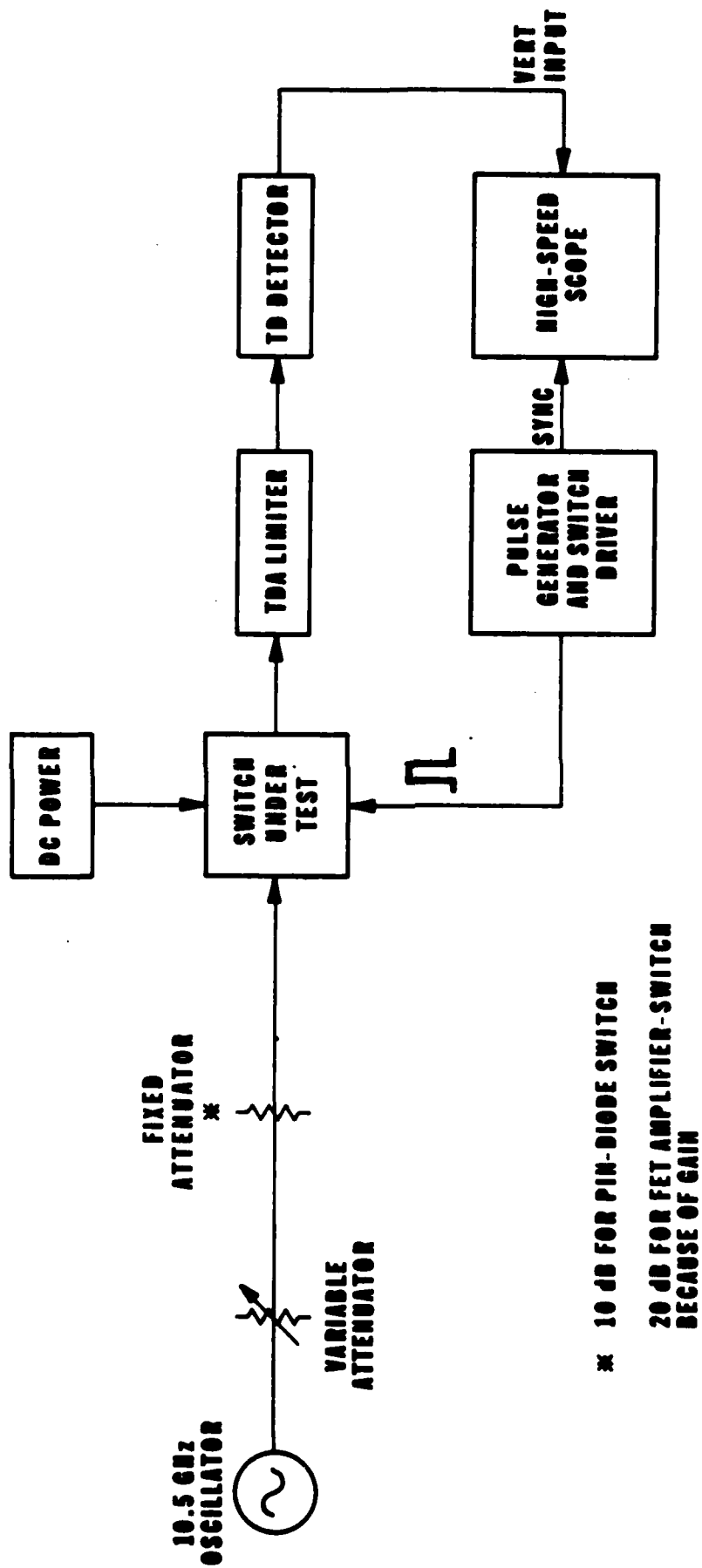
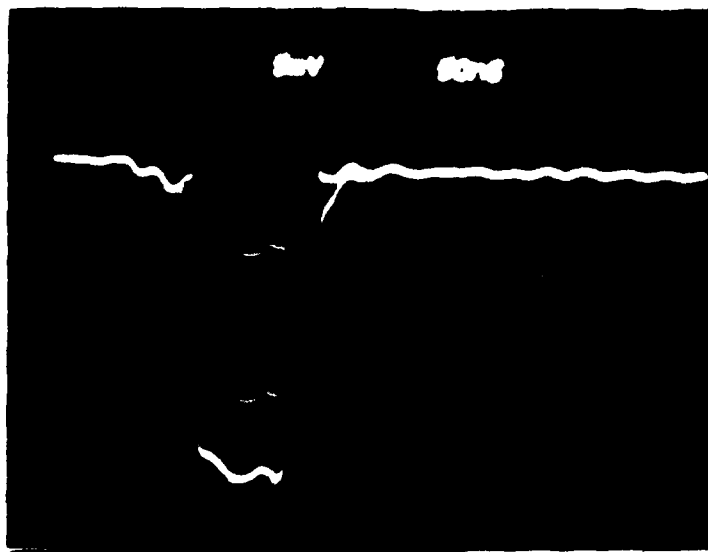
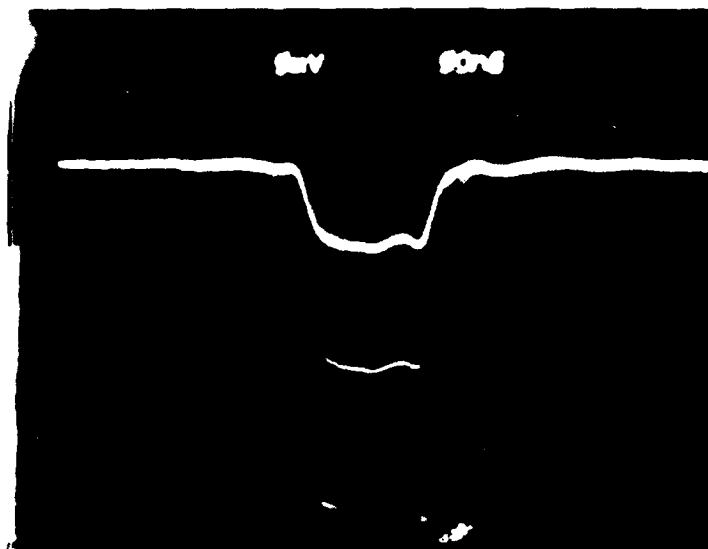


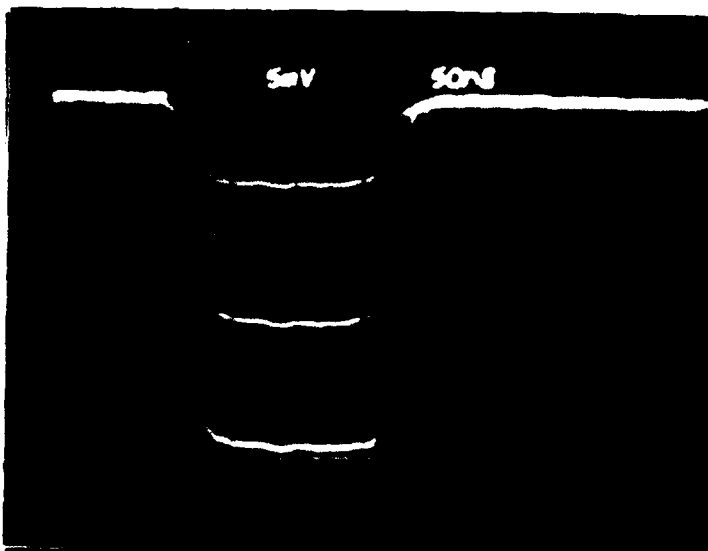
FIGURE 21. SATURATED DETECTOR TEST SET UP FOR SWITCH EVALUATION.



Alpha MT 3086 PIN-Diode Switch
Driven by HP1900A Pulse
Generator



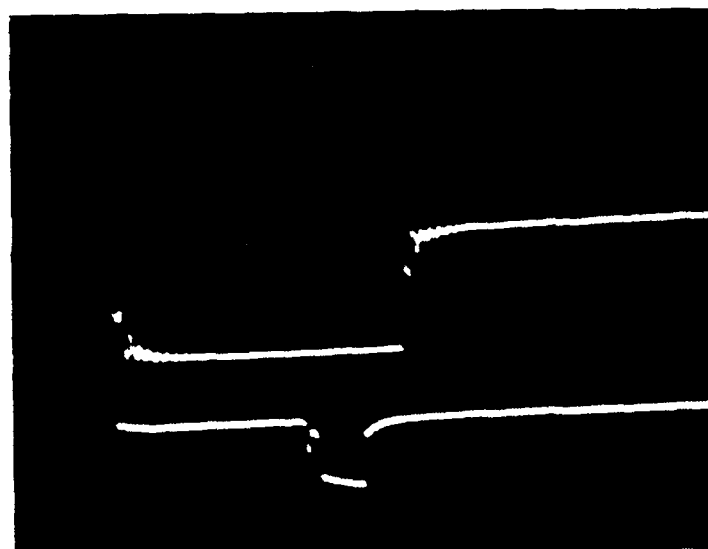
HP 8736B PIN-Diode Switch
Driven by Modulator HP 8403A



FET Amplifier-Switch S/N 1

FIGURE 22. COMPARISON OF SIMULATION PULSES PRODUCED BY PIN-DIODE SWITCHES AND
AN FET AMPLIFIER-SWITCH

GATED SPECTRUM GENERATED BY FET SWITCH



Oscilloscope
Display

ON

FET Switch Pulse

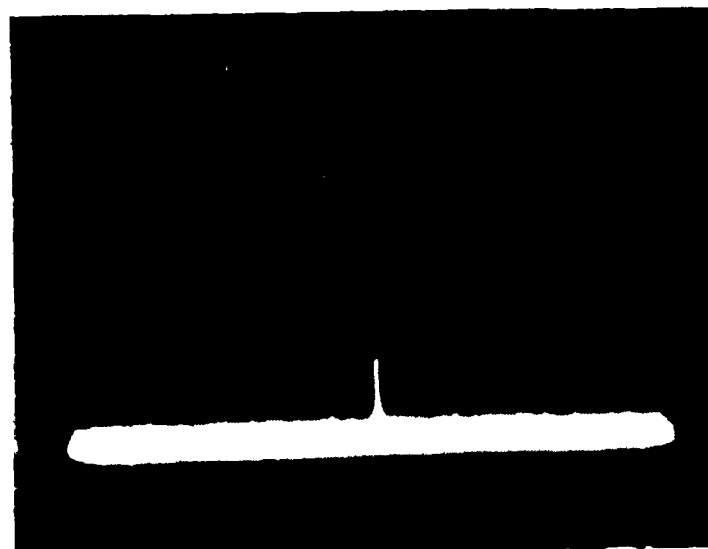
OFF

OFF

Spectrum Analyzer
Gate

ON

200 ns/div.

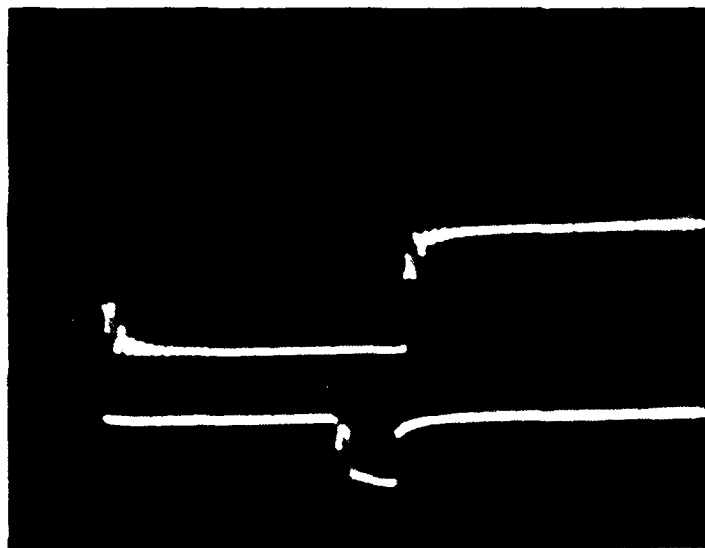


Spectrum Analyzer
Display

30 MHz/div.
 $F_c = 6 \text{ GHz}$

FIGURE 23. GATE CENTERED 200 ns BEFORE FET SWITCH PULSE

GATED SPECTRUM GENERATED BY FET SWITCH



Oscilloscope
Display

ON

FET Switch Pulse

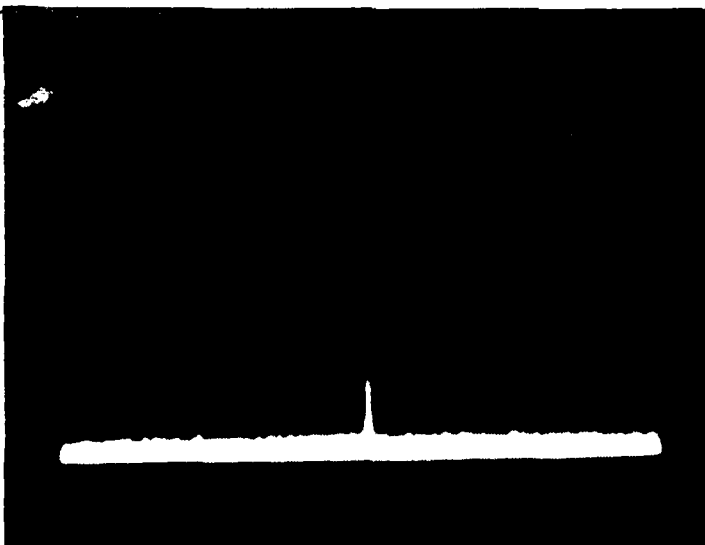
OFF

OFF

Spectrum Analyzer
Gate

ON

200 ns/div.

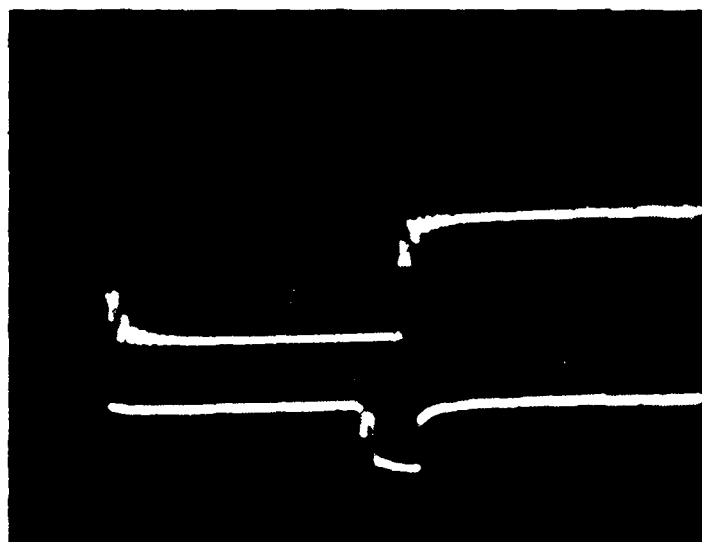


Spectrum Analyzer
Display

30 MHz/div.
 $F_c = 6 \text{ GHz}$

FIGURE 24. GATE CENTERED 100 ns BEFORE FET SWITCH PULSE

GATED SPECTRUM GENERATED BY FET SWITCH



Oscilloscope
Display

ON

FET Switch Pulse

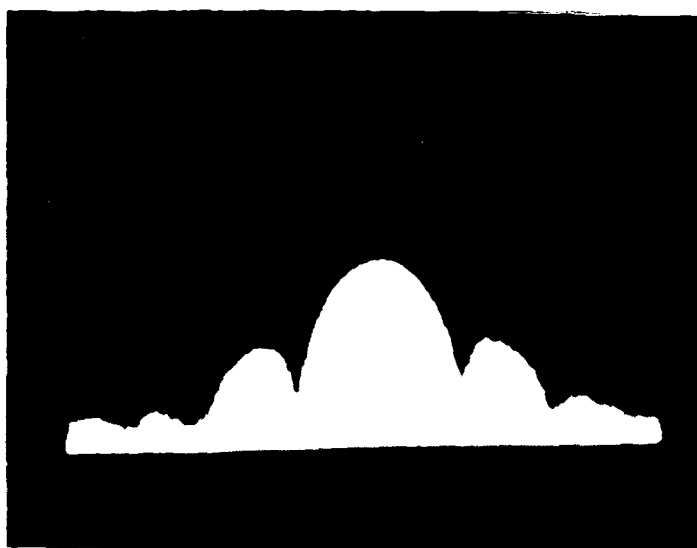
OFF

OFF

Spectrum Analyzer
Gate

ON

200 ns/div.

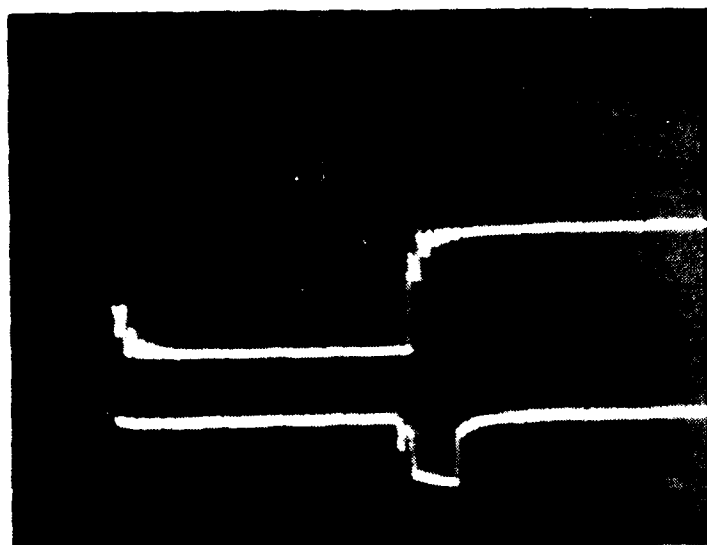


Spectrum Analyzer
Display

30 MHz/div.
 $F_c = 6 \text{ GHz}$

FIGURE 25. GATE CENTERED ON START OF FET SWITCH PULSE

GATED SPECTRUM GENERATED BY FET SWITCH



Oscilloscope
Display

ON

OFF

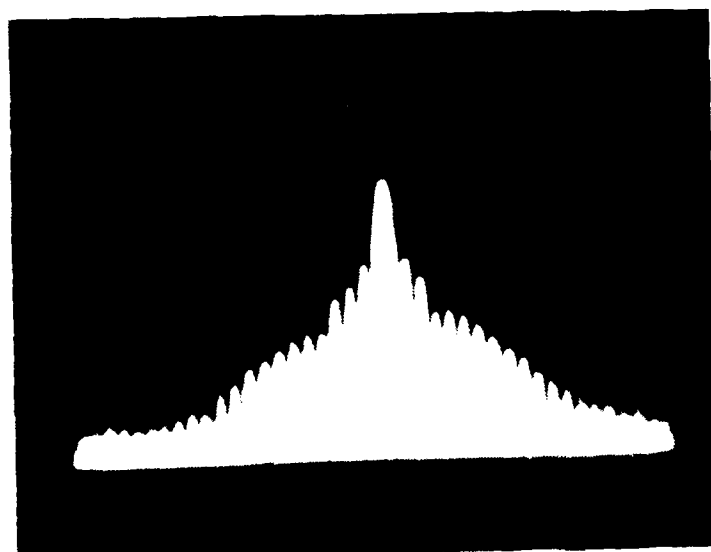
OFF

ON

FET Switch Pulse

Spectrum Analyzer
Gate

200 ns/div.

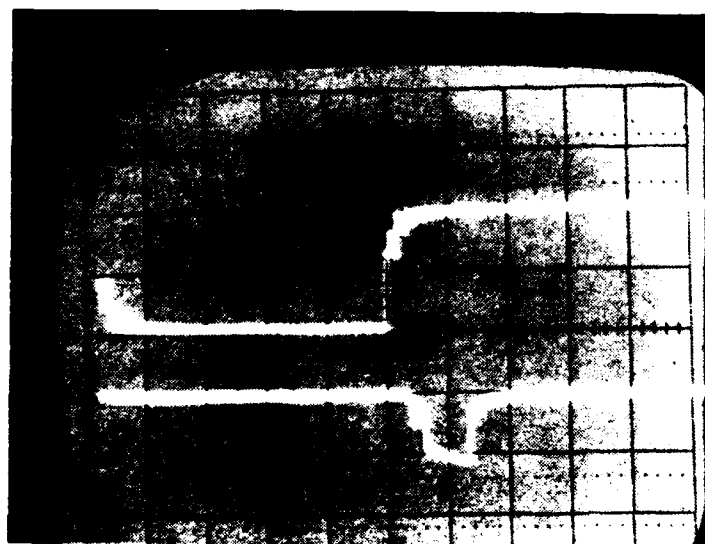


Spectrum Analyzer
Display

30 MHz/div.
 $F_c = 6$ GHz

FIGURE 26. GATE CENTERED 100 ns AFTER FET SWITCH PULSE

GATED SPECTRUM GENERATED BY FET SWITCH



Oscilloscope
Display

ON

FET Switch Pulse

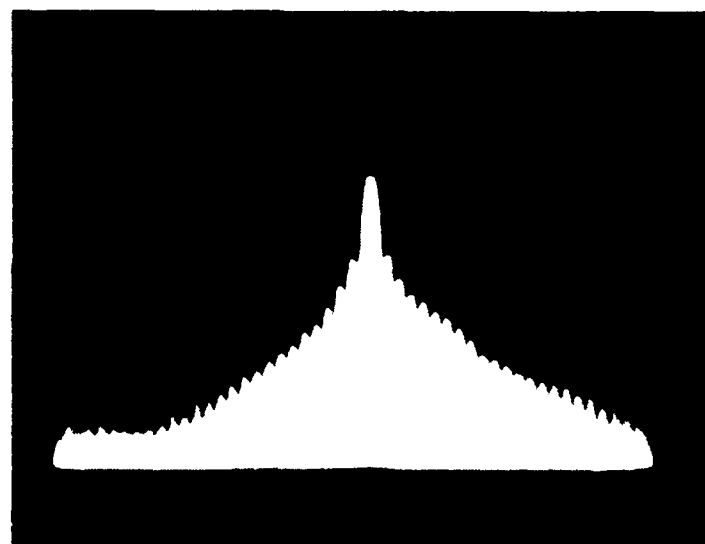
OFF

OFF

Spectrum Analyzer
Gate

ON

200 ns/div.



Spectrum Analyzer
Display

30 MHz/div.
 $F_c = 6 \text{ GHz}$

FIGURE 27. GATE CENTERED 200 ns AFTER FET SWITCH "ON" PULSE

END

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